Preliminary Program of APCCAS 2020

Last update: 13 November 2020

Time	Virtual Room 1	Virtual Room 2
Tuesday, December 8		
09:00-09:30	O1: *Opening Session*	
09:30-10:20	K1: *Keynote 1*	
10:30-12:10	A1: *Analog and Mixed-Signal I*	D1: *Digital Circuits and Systems I*
14:00-15:40	A2: *Analog and Mixed-Signal II*	D2: *Digital Circuits and Systems II*
16:00-18:00	A3: *Analog and Mixed-Signal III*	C1: *Communication Circuits and Systems*
Wednesday, December 9		
09:00-09:50	K2: *Keynote 2*	
10:00-11:00	SI1: *Sensors and Interfaces*	PA1: *PrimeAsia 2020 - I*
11:00-12:00	D3: *Digital Circuits and Systems III*	PA2: *PrimeAsia 2020 - II*
14:00-15:40	D4: *Digital Circuits and Systems IV*	V1: *Visual Signal Processing and Communications*
16:00-18:00	N1: *Neural Networks and Neuromorphic Engineering*	CS1: *Circuits and Systems*
Thursday, December 10		
09:00-11:00	S1: *Digital Signal Processing*	M1: *Multimedia Systems and Applications*
11:00-12:00	C: *Closing session*	

Note: Time and date are in Vietnam time zone (GMT+7)

Information on how to prepare and enter the virtual room will be updated later.

Note 2: Authors and presenters must check their information in this preliminary program and inform us via email: khanh.n.dang@vnu.edu.vn if mistakes or typos are founded.

Tuesday, December 8

O1: Opening Session

9:00 **Opening session**
Rooms: Virtual Room 1, Virtual Room 2

K1: Keynote 1

Rooms: Virtual Room 1, Virtual Room 2

9:30 Hardware Attack and Assurance with Machine Learning: A Security Threat to Circuits and Systems

Prof. Bah-Hwee Gwee (Nanyang Technological University, Singapore)

A1: Analog and Mixed-Signal I

Virtual Room 1

10:30 ***A 16-channel 50MS/s 14bit Pipelined-SAR ADC for Integrated Ultrasound Imaging Systems***
Yimin Wu, Jingchao Lan, Min Chen, Fan Ye and Junyan Ren (Fudan University, China)

10:50 ***An Area-Power-Efficient AFE with NS-SAR ADC For High-Frequency Ultrasound Applications***
Yimin Wu, Shuai Li, Longheng Luo, Fan Ye and Junyan Ren (Fudan University, China)

11:10 ***A Two-step SAR ADC with Synchronous DEM Calibration Achieving Up to 15% Power Reduction***
Zhechong Lan (Xi'an Jiaotong University, China); Li Dong, Xixin Jing and Liheng Liu (Xi'an Jiaotong University, China); Ken Li (Xi'an Jiaotong University, China); Ziyan Shen and Zhiming Li (Xi'an Jiaotong University, China); Li Geng (Xi'an Jiaotong University, China)

11:30 ***Low power PMIC with two hybrid converters for TEG application***
Thinh Tran-Dinh, Hieu Minh Pham, Bac Phuong Dao and Hien Hoang-Thi (Hanoi University of Science and Technology, Vietnam); Loan Pham-Nguyen (Hanoi University of Science and Technology & School of Electronics and Telecommunications, Vietnam); Sang-Gug Lee (Korea Advanced Institute of Science and Technology (KAIST), Korea (South)); Hanh-Phuc Le (University of California San Diego, USA)

11:50 ***A Spur-Free Low-Complexity Hybrid Nested Bus-Splitting/SP-MASH Digital Delta-Sigma Modulator***
Tieu Khanh Luong (Viettel High-Tech Industries Corporation, Vietnam); Hong Hanh Hoang and Hoang-Anh Nguyen-Minh (Viettel High-Tech Industries Corporation (VHT), Vietnam); Dang Cong Bui (Viettel High-Tech Industries Corporation, Vietnam); Viet-Son Bui (Viettel High-Tech Industries Corporation (VHT), Vietnam); Kien Nguyen (Viettel IC, Vietnam)

D1: Digital Circuits and Systems I

Virtual Room 2

10:30 ***ECC processor over the Koblitz curves with τ-NAF Converter and Square-Square-Add Algorithm***

Ting Wang and Tsung-Te Liu (National Taiwan University, Taiwan)

10:50 ***Efficient FPGA design for Convolutions in CNN based on FFT-pruning***

Liulu He (Nanjing University & School of Electronic Science and Engineering, China); Xiaoru Xie (Nanjing University & School of Electronic Science and Engineering, China); Jun Lin and Zhongfeng Wang (Nanjing University, China)

11:10 ***A DLL-based Body Bias Generator for Minimum Energy Operation with Independent P-well and N-well Bias***

Kentaro Nagai, Jun Shiomi and Hidetoshi Onodera (Kyoto University, Japan)

11:30 ***A Lightweight AEAD encryption core to secure IoT applications***

Nguyen Ngo Doanh and Bui Duy Hieu (Vietnam National University, Hanoi, Vietnam); Xuan-Tu Tran (VIetnam National University, Hanoi, Vietnam)

A2: Analog and Mixed-Signal II

Virtual Room 1

14:00 ***A Low-Power Low-Noise Dynamic Comparator With Latch-Embedding Floating Amplifier***

Ziwei Li, Wenbin He, Fan Ye and Junyan Ren (Fudan University, China)

14:20 ***Capacitive recombination calibration method to improve the performance of SAR ADC***

Hua Fan (University of Electronic Science and Technology of China, China)

14:40 ***A Single-Stage Delay-Tuned Active Rectifier for Constant-Current Constant-Voltage Wireless Charging***

Xianglong Bai and Fangyu Mao (University of Macau, China); Yan Lu (University of Macau, Macao); Chenchang Zhan (Southern University of Science and Technology, China); Rui P. Martins (University of Macau, Macao)

15:00 ***Design of SRAM cell using Voltage Lowering and Stacking Techniques for Low Power Applications***

Jitendra Kumar Mishra (Indian Institute of Information Technology, Allahabad, India); Prasanna Kumar Misra and Manish Goswami (Indian Institute of Information Technology, India)

15:20 ***Dynamic Reduction of Power Consumption in Direct-RF Sampling Receivers with Variable Decimation***

Yuka Nakamatsu and Takao Kihara (Osaka Institute of Technology, Japan)

D2: Digital Circuits and Systems II

Virtual Room 2

14:00 ***High-Performance Implementation of Adaptive IQ Mismatch Compensator in Direct-Conversion Transceiver***

Toan Van Nguyen (Viettel High Technology Industries Corporation (VHT), Viettel Group, Vietnam); Viet-Son Bui (Viettel High-Tech Industries Corporation (VHT), Vietnam); Kien Nguyen (Viettel IC, Vietnam)

14:20 ***Stress evolution analysis of EM-induced void growth for multi-segment interconnect wires***

Zaiyong Liu, Haibao Chen and Tianshu Hou (Shanghai Jiao Tong University, China)

14:40 ***Performance Analysis of Non-Profiled Side Channel Attacks Based on Convolutional Neural Networks***

Ngoc-Tuan Do and Van-Phuc Hoang (Le Quy Don Technical University, Vietnam); Sang Van Doan (Vietnam Naval Academy, Vietnam & ICT CRC, Kumoh National Institute of Technology, Korea (South))

15:00 ***An Energy-Efficient Time-Domain Binary Neural Network Accelerator with Error-Detection in 28nm CMOS***

Yuxuan Du, Xinchao Shang and Weiwei Shan (Southeast University, China)

15:20 ***Low-Power Implementation of a High-Throughput Multi-core AES Encryption Architecture***

Pham- Khoi Dong (VNU University of Engineering and Technology, Vietnam); Hung K. Nguyen (VNU University of Engineering and Technology, Vietnam); Van-Phuc Hoang (Le Quy Don Technical University, Vietnam); Xuan-Tu Tran (VIetnam National University, Hanoi, Vietnam)

A3: Analog and Mixed-Signal III

Virtual Room 1

16:00 ***Sub-Sampling Phase-Locked Loop with Ultra-mini Dead Zone For Locking Time Reduction***

Yeqing Wang and Zhouchen Ma (Shanghai Jiao Tong University, China); Lei Zhang and Zongmin Wang (Beijing Micro-electronic Technology Institute, China); Yan Liu and Jian Zhao (Shanghai Jiao Tong University, China)

16:20 ***Low Power Reference Voltage Buffer and High Density Unit capacitor in a 12b 200MS/s SAR ADC***

Wenbin He, Ziwei Li, Fan Ye and Junyan Ren (Fudan University, China)

16:40 ***Open Top Socketed Evaluation Board for Bench Test and Fault Localization on GaAs RF Device***

Alex Marionne A. del Castillo (Analog Devices Inc., Philippines); Ramon Garcia and Febus Reidj G. Cruz (Mapua University, Philippines)

17:00 ***A Self-coupled DT MASH ΔΣ Modulator with High Tolerance to Noise Leakage***
Gaofeng Tan (Shanghai Jiao Tong University, China); Haolin Lu (Tianjin University, China); Xinyu Qin, Jiliang Zhang, Jingying Zhang and Yan Liu (Shanghai Jiao Tong University, China); Liang Qi (Shanghai Jiaotong University, China)

17:20 ***"Truth from Practice, Learning beyond Teaching" Exploration in teaching Analog Integrated Circuit***
Hua Fan (University of Electronic Science and Technology of China, China)

C1: Communication Circuits and Systems

Virtual Room 2

16:00 ***100 MHz Random Number Generator Design Using Interleaved Metastable NAND/NOR Latches***
Chua-Chin Wang and Shao-Wei Lu (National Sun Yat-Sen University, Taiwan)

16:20 ***A RISC-V SoC for Mobile Payment Based on Visible Light Communication***
Xinchao Zhong, Chiu Wing Sham and Longyu Ma (The University of Auckland, New Zealand)

16:40 ***Digital Phase Estimation through an I/Q Approach for Angle of Arrival Full-Hardware Localization***
Antonello Florio, Gianfranco Avitabile and Giuseppe Coviello (Politecnico di Bari, Italy)

17:00 ***Frequency-Tunable Quasi-Elliptic Filter Using Liquid Metal***
Matthew D Brown and Carlos E. Saavedra (Queen's University, Canada)

> End of Day 1

Wednesday, December 9

K2: Keynote 2

Rooms: Virtual Room 1, Virtual Room 2

9:00 IoT and Blockchain: Technologies, Challenges, and Applications

Prof. Ren Ping Liu (University of Technology Sydney, Australia)

SI1: Sensors and Interfaces

Virtual Room 1

10:00 ***Damage Position Identification of Wooden House Model Using Machine Learning***
Kohei Koike, Kenta Suzuki, Mengnan Ke, Kenjiro Mori, Takumi Ito and Takayuki Kawahara (Tokyo University of Science, Japan)

10:20 ***A Highly Linear Amp-Less Interface Circuit for Capacitive Sensors with ΔΣ C-DAC***
Yuya Maekawa, Shuya Nakagawa and Hiroki Ishikuro (Keio University, Japan)

PA1: PrimeAsia 2020 - I

Virtual Room 2

10:00 ***A High-Performance Symmetric Hybrid Form Design for High-Order FIR Filters***
Jinghao Ye, Masao Yanagisawa and Youhua Shi (Waseda University, Japan)

10:20 ***Low-Noise Amplifier with Wideband Feedforward Linearisation for Mid-Band 5G Receivers***
Sarmad Ozan, Manish Nair, Tommaso Cappello and Mark Beach (University of Bristol, United Kingdom (Great Britain))

10:40 ***Random Number Generator Based on Miniature Microbial Fuel Cells***
Celal Erbay (TUBITAK - Informatics and Information Security Research Center, Turkey); Salih Ergun (TUBITAK - Informatics and Information Security Research Center, Turkey & ERGTECH Research Center, Switzerland)

D3: Digital Circuits and Systems III

Virtual Room 1

11:00 ***A Light-Weight Timing Resilient Scheme for Near-Threshold Efficient Digital ICs***
Xuemei Fan, Hongwei Li, Qiang Li, Liu Hao and Shengli Lu (Southeast University, China)

11:20 ***An Efficient Accelerator of the Squaring for the Verifiable Delay Function Over a Class Group***
Danyang Zhu, Yifeng Song, Jing Tian and Zhongfeng Wang (Nanjing University, China); Haobo Yu (Snap Inc., USA)

11:40 ***Fast Permutation Architecture on Encrypted Data for Secure Neural Network Inference***
Xiao Hu, Jing Tian and Zhongfeng Wang (Nanjing University, China)

PA2: PrimeAsia 2020 - II

Virtual Room 2

11:00 ***3D-Modeling Dataset Augmentation for Underwater AUV Real-time Manipulations***
Chua-Chin Wang, Chia-Yi Huang, Chu-Han Lin, Chia-Hung Yeh, Guan-Xian Liu and Yu-Cheng Chou (National Sun Yat-Sen University, Taiwan)

11:20 ***Automatic Tongue Image Segmentation Based on Thresholding and an Improved Level Set Model***
Hongyu Gu and Zhecheng Yang (Tsinghua University, China); Hong Chen (Tsinghua, China)

11:40 ***Design and manufacture power pre-amplifier module for transmitter of ground station at S-band***
Ha Thi Bui (VietNam Space Center & VietNam National Satellite Center, Vietnam)

D4: Digital Circuits and Systems IV

Virtual Room 1

14:00 ***An Energy Operating System Adaptive for The Sustainable And Green Energy***

Yen-Bor Lin, Chih-Chieh Ma, Chong-Cheng Hsu, Ting-Chia Ou, Tsung-Chieh Cheng and Wen-Fu Chen (Institute of Nuclear Energy Research, Atomic Energy Council, Executive Yuan, Taiwan)

14:20 ***High Efficient Early-Complete Brute Force Elimination Method for Security Analysis of Camouflage IC***

Weng-Geng Ho, Chuan-Seng Ng, Nay Aung Kyaw, Kyaw Zwa Lwin Ne and Kwen Siong Chong (Nanyang Technological University, Singapore); Bah Hwee Gwee (NTU, Singapore)

14:40 ***An Efficient FPGA Accelerator Optimized for High Throughput Sparse CNN Inference***

Jiayu Wen, Yufei Ma and Zhongfeng Wang (Nanjing University, China)

15:00 ***Copper Coin over Thermal Via in PCB for Thermal Management of 12 W***

Marcus Miguel Vicedo (Analog Devices Inc., Philippines); Febus Reidj G. Cruz and Ramon Garcia (Mapua University, Philippines)

V1: Visual Signal Processing and Communications

Virtual Room 2

14:00 ***Fast Object Detection on the Road***

T. Hui Teo (Singapore University of Technology and Design, Singapore); Yi Shu Tan (Singapore University of Technology & Design, Singapore)

14:20 ***Graph Saliency Network: Using Graph Convolution Network on Saliency Detection***

Heng-Sheng Lin, Jian-Jiun Ding and Jin-Yu Huang (National Taiwan University, Taiwan)

14:40 ***Improved Angle Freeman Chain Code Using Improved Adaptive Arithmetic Coding***

Ji-Ting Wu and Jian-Jiun Ding (National Taiwan University, Taiwan)

15:00 ***Using Fully Connected and Convolutional Net for GAN-Based Face Swapping***

Bo-Shue Lin, Ding-Wen Hsu, Chin-Han Shen and Hsu-Feng Hsiao (National Chiao Tung University, Taiwan)

15:20 ***Dilated Residual Convolutional Neural Networks for Low-Dose CT Image Denoising***

Thanh-Trung Nguyen (University of Engineering and Technology, VNU & Thainguyen Universisty of Information and Communication Technology, Vietnam); Dinh Hoan Trinh (Université de Bourgogne & ImViA, France); Nguyen Linh Trung (Vietnam National University, Hanoi, Vietnam); Tran Thi Thuy Quynh (VNU University of Engineering and Technology, Vietnam); Luu Manh Ha (AVITECH & FET, University of Technology and Engineering, VNU, Hanoi, Vietnam & Erasmus MC, Rotterdam, The Netherlands)

N1: Neural Networks and Neuromorphic Engineering

Virtual Room 1

16:00 ***Design of an 45nm NCFET Based Compute-in-SRAM for Energy-Efficient Machine Learning Applications***

Chia-Heng Lee, Ying-Tuan Hsu, Tsung-Te Liu and Tzi-Dar Chiueh (National Taiwan University, Taiwan)

16:20 ***Improvement of Generalization performance for Timber Health Monitoring using Machine Learning***

Kenta Suzuki, Kohei Koike, Mengnan Ke, Kenjiro Mori, Takumi Ito and Takayuki Kawahara (Tokyo University of Science, Japan)

16:40 ***LBFP: Logarithmic Block Floating Point Arithmetic for Deep Neural Networks***

Chao Ni (Nanjing University & School of Electronic Science and Engineering, China); Jinming Lu, Jun Lin and Zhongfeng Wang (Nanjing University, China)

17:00 ***A Calibration Scheme for Nonlinearity of the SAR-Pipelined ADCs Based on a Shared Neural Network***

Min Chen, Yimin Wu, Jingchao Lan, Chixiao Chen, Fan Ye and Junyan Ren (Fudan University, China)

17:20 ***A lightweight Max-Pooling method and architecture for Deep Spiking Convolutional Neural Networks***

Duy-Anh Nguyen (VNU University of Engineering and Technology, Vietnam); Xuan-Tu Tran (VIetnam National University, Hanoi, Vietnam); Khanh N. Dang (Vietnam National University, Hanoi, Vietnam); Francesca Iacopi (University of Technology Sydney, Vietnam)

CS1: Circuits and Systems

Virtual Room 2

16:00 ***ReRAM Device and Circuit Co-Design Challenges in Nano-scale CMOS Technology***

Lu Lu, Ju Eon Kim, Vishal Sharma and Tony Tae Hyoung Kim (Nanyang Technological University, Singapore)

16:20 ***Lossless EEG Compression Algorithm Based on Semi-Supervised Learning for VLSI Implementation***

Yi-Hong Chen, Yan-Ting Liu and Tsun-Kuang Chi (Chung Yuan Christian University, Taiwan); Chiung-An Chen (Ming Chi University of Technology, Taiwan); Yih-Shyh Chiou (Chung Yuan Christian University, Taiwan); Ting-Lan Lin (National Taipei University of Technology, Taiwan); Shih-Lun Chen (Chung Yuan Christian University, Taiwan)

16:40 ***A 72-nW 440-mV Time Register Using Stacked-NMOS-Switched Gated Delay Cell in Biomedical Applications***

Guowei Chen, Dang Bui and X. Yu (Graduate School of Nagoya University, Japan); Md. Zahidul Islam (Graduate School of Engineering, Nagoya University, Japan); A. Kobayashi (Graduate School of Nagoya University, Japan); Kiichi Niitsu (Nagoya University, Japan)

17:00 ***Random Number Generator Based on Skew-tent Map and Chaotic Sampling***

Salih Ergun (TUBITAK - Informatics and Information Security Research Center, Turkey & ERGTECH Research Center, Switzerland); Sercan Tanriseven (ERGTECH Research Center, Switzerland)

17:20 ***Experimental Cryptanalysis of No-equilibrium Chaotic System Based Random Number Generator***

Burak Acar and Tufan C. Karalar (Istanbul Technical University, Turkey)

> End of Day 2

Thursday, December 10

S1: Digital Signal Processing

Virtual Room 1

9:00 ***Real-Time Hardware Implementation of 3D Sound Synthesis***
Sathwik GS, Barun Kumar Acharya and Bilal Ali (National Institute of Technology Karnataka Surathkal, India); Deepu Sp (National Institute of Technology Karnataka, Surathkal, India); Sumam David S. (National Institute of Technology Karnataka, India)

9:20 ***Axial Resolution Enhancement of Light Sheet Microscopy via Two Light Sheet***
VanNhu Le, MinhNghia Pham and Vandang Hoang (Le Quy Don Technical University, Vietnam)

9:40 ***Revisit to Floating-Point Division Algorithm Based on Taylor-Series Expansion***
Jianglin Wei, Anna Kuwana and Haruo Kobayashi (Gunma University, Japan); Kazuyoshi Kubo (Oyama National College of Technology, Japan)

10:00 ***Missing Temperature Data Recovery Methods Based on Smoothness, Bandlimitedness and Sparseness Priors***
Chien-Cheng Tseng (National Kaohsiung University of Science and Technology, Taiwan); Su-Ling Lee (Chang-Jung Christian University, Taiwan)

M1: Multimedia Systems and Applications

Virtual Room 2

9:00 ***Learning Based Age Estimation Using Joint Loss and Facial Landmarks***
Min Chen Hsu and Jian-Jiun Ding (National Taiwan University, Taiwan)

9:20 ***Learning Enriched Features for Video Deonising with Convolutional Neural Network***
Xianfeng Tang and Peining Zhen (Shanghai Jiao Tong University, China); Ming Kang (Galaxycore Shanghai Limited Corporation, China); Hang Yi and Wei Wang (Beijing Institute of Astronautical Systems Engineering, China); Haibao Chen (Shanghai Jiao Tong University, China)

9:40 ***Histogram of Oriented Gradients Feature Extraction Without Normalization***
Ling Zhang, Wei Zhou and Xin Lou (ShanghaiTech University, China)

C: Closing session

Rooms: Virtual Room 1, Virtual Room 2

11:00 Closing speech, Best paper award, announcements

> End of Day 3