

## PROGRAM AT A GLANCE

Time	Virtual Room 1	Virtual Room 2
Tuesday, December 8, 2020		
09:00-09:30	O1: Opening Session	
09:30-10:20	K1: Keynote 1 - Prof. Bah-Hwee Gwee (Nanyang Technological University, Singapore)	
10:30-12:10	A1: Analog and Mixed-Signal I	D1: Digital Circuits and Systems I
14:00-15:40	A2: Analog and Mixed-Signal II	D2: Digital Circuits and Systems II
16:00-18:00	A3: Analog and Mixed-Signal III	C1: Communication Circuits and Systems
Wednesday, December 9, 2020		
09:00-09:50	K2: Keynote 2 - Prof. Ren Ping Liu (University of Technology Sydney, Australia)	
10:00-11:00	SI1: Sensors and Interfaces	PA1: PrimeAsia 2020 - I
11:00-12:00	D3: Digital Circuits and Systems III	PA2: PrimeAsia 2020 - II
14:00-15:40	D4: Digital Circuits and Systems IV	V1: Visual Signal Processing and Communications
16:00-18:00	N1: Neural Networks and Neuromorphic Engineering	CS1: Circuits and Systems
Thursday, December 10, 2020		
09:00-11:00	S1: Digital Signal Processing	M1: Multimedia Systems and Applications
11:00-12:00	C: Closing session	

Note: Time and date are in Vietnam time zone (GMT+7)

## MESSAGE FROM GENERAL CHAIR

Warmly welcome to 16th IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS 2020) and the 2020 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia 2020)!

On behalf of the organizing committee, it is our pleasure to cordially welcome and invite you to the APCCAS 2020 and the PrimeAsia 2020, to be held in Ha Long Bay, Vietnam and virtually on the Internet, during December 8-10, 2020. The IEEE APCCAS is one of the major conferences sponsored by the IEEE Circuits and Systems (CAS) Society and has been held in Asia-Pacific countries, where APCCAS 2020 is the 16th annual conference in the series. APCCAS is the international forum for researchers, scientists, educators, students and engineers to discuss and exchange experiences with the aim to stimulate and enhance the research and development in the areas that are related to Circuits and Systems. The IEEE PrimeAsia is an initiative of the IEEE Circuits and Systems Society in Asia and Pacific Region for engaging students. It aims to provide an opportunity for postgraduate students (Masters and PhD) to present their research works and to interact with scientists and engineers in the research community and industry.

Ha Long Bay is a UNESCO World Heritage site of Vietnam and is appreciated by visitors in a large range of attractions. Please make sure to take this opportunity to visit and get around Ha Long with your own eyes (if possible). Due to the Covid-19 pandemic, the conference committee decided to organize the conference with both face-to-face and online modes with limited services, based on most authors' appeal and health consideration after careful discussion. We would like to thank all participants for sharing with us in this difficult period.

Finally, as the General Chair of the Conference, I would like to express my sincere thanks to all sponsors, keynote/invited speakers, session chairs, committee members, authors, and participants to build this memorable and informative conference. We hope that all of you will enjoy this special conference, embrace technology & innovation, and hope that the face-to-face participants have safe stays in Ha Long Bay.

**Xuan-Tu Tran**

Vietnam National University, Hanoi

General Chair,

APCCAS 2020 & PrimeAsia 2020

## MESSAGE FROM TPC CO-CHAIR

On behalf of the technical program committee of the 2020 IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS 2020), we are sincerely delighted to welcome all of you to the IEEE APCCAS 2020 in Ha Long Bay, Vietnam. The IEEE APCCAS has been held in Asia-Pacific countries is one of the flagship conferences sponsored by the IEEE Circuits and Systems (CAS) Society. APCCAS 2020, which is the 16<sup>th</sup> edition of the conference series, is held in conjunction with the 2020 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia).

IEEE APCCAS 2020 and PrimeAsia 2020 attracted 111 submissions from 27 different countries around the world. After a rigorous blind review process, we have carefully selected and accepted a total number of 65 papers to be included in the technical program: 59 papers for APCCAS2020 and 6 papers for PrimeAsia 2020. The geographical distribution of the accepted papers is as follows: 58 are from Asia-Pacific, 5 are from Europe, 1 are from Pacific Ocean, and 1 is from North America. The joint technical program includes 2 invited plenary sessions, 2 PrimeAsia sessions, and 14 regular APCCAS lecture sessions.

This year we are very pleased to have two distinguished keynotes. The first plenary talk by Professor Bah-Hwee Gwee will address the current developments and future challenges of hardware attack and assurance with machine learning. In the second plenary lecture, Professor Ren Ping Liu will cover the technologies, challenges, and applications of IoT and blockchain.

The success of the technical program is a result of the conscientious volunteer work of the technical program committee and reviewers. The technical program committee consists of 15 track chairpersons who conducted the review process with the help of 44 TPC members and more than 200 reviewers from many different countries. We would like to express our sincere appreciation to all the track chairpersons and the reviewers for their devoted contributions.

Finally, we would like to thank all the authors and contributors to the success of APCCAS 2020. We sincerely wish that all the attendees and participants will enjoy the technical programs of the IEEE APCCAS 2020 and have a memorable time and experience in Vietnam!

### TPC co-Chairs

Lan-Da Van, National Chiao Tung University, Taiwan  
Khanh N. Dang, Vietnam National University, Hanoi, Vietnam  
Ingrid Verbauwhede, KU Leuven, Belgium  
Van-Phuc Hoang, Le Quy Don Technical University, Vietnam

Rooms: **Virtual Room 1, Virtual Room 2**

**9:30 (GMT+7) Tuesday, December 8**

**Title: Hardware Attack and Assurance with Machine Learning: A Security Threat to Circuits and Systems**



**Prof. Bah-Hwee Gwee**

**Nanyang Technological University, Singapore**

**Abstract:** Banking, defence applications and cryptosystems often demand security features, including cryptography, tamper resistance, stealth, and etc., by means of hardware approaches and/or software approaches to prevent data leakages. The hardware physical attacks or commonly known as side channel attacks have been employed to extract the secret keys of the encrypted algorithms implemented in hardware devices by analyzing their physical parameters such as power dissipation, electromagnetic interference and timing information. Altered functions or unauthorized modules may be added to the circuit design during the shipping and manufacturing process, bringing in security threats to the deployed systems. In this presentation, we will discuss hardware assurance from both device level and circuit level, and present how machine learning techniques can be utilized. At the device level, we will first provide an overview of the different cryptography algorithms and present the side channel attacks, particularly the powerful Correlation Power Analysis (CPA) and Correlation Electromagnetic Analysis (CEMA) with a leakage model that can be used to reveal the secret keys of the cryptosystems. We will then discuss several countermeasure techniques and present how highly secured microchips can be designed based on these techniques. At the circuit level, we will provide an overview of manufactured IC circuit analysis through invasive IC delayering and imaging. We then present several machine learning techniques that can be efficiently applied to the retrieval of circuit contact points and connections for further netlist/functional analysis.

**Bibliography:** Dr Bah-Hwee Gwee received his B.Eng degree from University of Aberdeen, UK, in 1990. He received his MEng and PhD degrees from Nanyang Technological University in 1992 and 1998 respectively. He was an Assistant Professor of School of EEE, NTU from 1999 to 2005. He is currently an Associate Professor in School of EEE, NTU. He has worked on a number of research projects with research grant amounting to S\$8m (~US\$5.7m). He was the principal investigator of the research projects from MoE Academic Research Tier-2 grant of S\$1.3m (~US\$860k), ASEAN-EU University Network Programme grant of €200k and the Defense Science Organization grant of S\$3.25m (~US\$2.32m). He was also the Co-Principal Investigator of NTU-Panasonic research collaboration amounting to S\$1m (~US\$800k) and DARPA project of ~US\$350k, Linkoping University – NTU joint research collaboration of S\$660k (~US\$400k), The Agency for Science, Technology and Research (A\*STAR) – PSF research project of S\$700k ((USD500k). His research interests include low power asynchronous IC design, Class-D amplifiers, digital signal processing and soft computing. He has published more than 100 technical papers, 6 patents (3 granted in USA) and started a Start-up Company in 2005.

He was the Chairman of IEEE-Singapore Circuits and Systems Chapter in 2005, 2006, 2013 and 2016. He is the Chairman of IEEE Circuits and Systems Society – DSPTC (2019-2020). He was the General Co-Chair of IEEE DSP 2018 and IEEE SOCC 2019. He was the organizing committee of the IEEE Bio-CAS 2004, IEEE APCCAS 2006 and the TPC Chair of International Symposium on Integrated Circuits (ISIC 2007, ISIC 2011 and ISIC 2016). He has also served as Associate Editors of a number of journals, including IEEE Transactions of Circuits and Systems II – Brief Express (2018-2019) and (2019-2020), IEEE Transactions of Circuits and Systems I – Regular Papers (2012-2013), IEEE Transactions of Circuits and Systems II – Brief

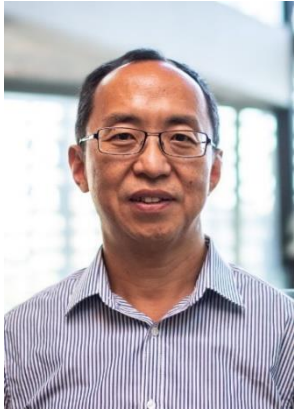
Express (2010-2011) and Journal of Circuits, Systems and Signal Processing (2007-2012). He was awarded Temasek Laboratories @ NTU Best Publication Award in 2012 and the Teaching Excellence Award (Year 3) in 2013. He was an IEEE Distinguished Lecture for Circuits and Systems Society in 2009-2010 and in 2017/2018. He was awarded the Singapore Defence Technology Prize in 2016.

K2: Keynote 2

Rooms: **Virtual Room 1, Virtual Room 2**

**9:00 (GMT+7) Wednesday, December 9**

**Title: IoT and Blockchain: Technologies, Challenges, and Applications**



**Prof. Ren Ping Liu**  
**University of Technology Sydney, Australia**

**Abstract:** The Internet of Things (IoT) is poised to transform our lives and unleash enormous economic benefit. In this talk, we discuss a wide range of IoT technologies and their applications, as well as the security and trust implications. Blockchain, a distributed ledger, was initially designed as a secure financial transaction tool. Remarkably, its cryptographic security benefits, such as user anonymity, decentralization, fault tolerance, transaction integrity and authentication, can be used to resolve security and trust issues of IoT.

In UTS, we are working with industry to develop next generation IoT and Blockchain technologies to achieve real time tracking and monitoring from production plants through export supply chains to overseas markets. A Blockchain enabled data platform has been developed to secure IoT data records, enable transparent and trusted data sharing. Smart contracts are developed to manage and automate commercial transactions following the commodity flows.

**Bibliography:** Bibliography: Ren Ping Liu is a Professor and Head of Discipline of Network and Cybersecurity at University of Technology Sydney. He was the co-founder and CTO of Ultimo Digital Technologies, developing IoT and Blockchain. Prior to that he was a Principal Scientist and Research Leader at CSIRO, where he led wireless networking research activities. Professor Liu is a certified network professional and full stack developer. He has delivered networking solutions to a number of government agencies and industry customers. His research interests include 5G, VANET, IoT, cybersecurity, and Blockchain. He has over 150 research publications and has supervised over 30 PhD students.

Professor Liu was the winner of NSW iAwards 2020 for leading the BeFAQT (Blockchain enabled Fish provenance And Quality Tracking) project. He was the winner of Australian Engineering Innovation Award 2012 and CSIRO Chairman's medal for his contribution in the Wireless Backhaul project. Professor Liu was the founding chair of IEEE NSW VTS Chapter and a Senior Member of IEEE. He served as Technical Program Committee chairs, Organising Committee chairs, and delivered keynote speeches in a number of IEEE Conferences and industry forums.

In this talk, we will discuss the benefits, limitations, and challenges of IoT and Blockchain. I will present some of our latest project results in IoT and Blockchain applications, including our award-winning project BeFAQT ([befaqt.com](http://befaqt.com)).

Tuesday, December 8

## O1: Opening Session

**9:00 Opening session**

Rooms: Virtual Room 1

## K1: Keynote 1

Rooms: **Virtual Room 1**

**Session chair:** Xuan-Tu Tran (Vietnam National University, Hanoi, Vietnam)

**9:30 Hardware Attack and Assurance with Machine Learning: A Security Threat to Circuits and Systems**

Prof. Bah-Hwee Gwee (Nanyang Technological University, Singapore)

## A1: Analog and Mixed-Signal I

**Virtual Room 1**

**Session chair:** Yong Chen (University of Macau, Macau, China)

**10:30 A 16-channel 50MS/s 14bit Pipelined-SAR ADC for Integrated Ultrasound Imaging Systems**

Yimin Wu, Jingchao Lan, Min Chen, Fan Ye and Junyan Ren (Fudan University, China)

**10:50 An Area-Power-Efficient AFE with NS-SAR ADC For High-Frequency Ultrasound Applications**

Yimin Wu, Shuai Li, Longheng Luo, Fan Ye and Junyan Ren (Fudan University, China)

**11:10 A Two-step SAR ADC with Synchronous DEM Calibration Achieving Up to 15% Power Reduction**

Zhechong Lan (Xi'an Jiaotong University, China); Li Dong, Xixin Jing and Liheng Liu (Xi'an Jiaotong University, China); Ken Li (Xi'an Jiaotong University, China); Ziyang Shen and Zhiming Li (Xi'an Jiaotong University, China); Li Geng (Xi'an Jiaotong University, China)

**11:30 Low power PMIC with two hybrid converters for TEG application**

Thinh Tran-Dinh, Hieu Minh Pham, Bac Phuong Dao and Hien Hoang-Thi (Hanoi University of Science and Technology, Vietnam); Loan Pham-Nguyen (Hanoi University of Science and Technology & School of Electronics and Telecommunications, Vietnam); Sang-Gug Lee (Korea Advanced Institute of Science and Technology (KAIST), Korea (South)); Hanh-Phuc Le (University of California San Diego, USA)

**11:50 A Spur-Free Low-Complexity Hybrid Nested Bus-Splitting/SP-MASH Digital Delta-Sigma Modulator**

Tieu Khanh Luong (Viettel High-Tech Industries Corporation, Vietnam); Hong Hanh Hoang and Hoang-Anh Nguyen-Minh (Viettel High-Tech Industries Corporation)



(VHT), Vietnam); [Dang Cong Bui](#) (Viettel High-Tech Industries Corporation, Vietnam); [Viet-Son Bui](#) (Viettel High-Tech Industries Corporation (VHT), Vietnam); [Kien Nguyen](#) (Viettel IC, Vietnam)

## D1: Digital Circuits and Systems I

### Virtual Room 2

**Session chair:** Lan-Da Van (National Chiao Tung University, Taiwan)

**10:30 ECC processor over the Koblitz curves with  $\tau$ -NAF Converter and Square-Square-Add Algorithm**

[Ting Wang](#) and [Tsung-Te Liu](#) (National Taiwan University, Taiwan)

**10:50 Efficient FPGA design for Convolutions in CNN based on FFT-pruning**

[Liulu He](#) (Nanjing University & School of Electronic Science and Engineering, China); [Xiaoru Xie](#) (Nanjing University & School of Electronic Science and Engineering, China); [Jun Lin](#) and [Zhongfeng Wang](#) (Nanjing University, China)

**11:10 A DLL-based Body Bias Generator for Minimum Energy Operation with Independent P-well and N-well Bias**

[Kentaro Nagai](#), [Jun Shiomi](#) and [Hidetoshi Onodera](#) (Kyoto University, Japan)

**11:30 A Lightweight AEAD encryption core to secure IoT applications**

[Nguyen Ngo Doanh](#) and [Bui Duy Hieu](#) (Vietnam National University, Hanoi, Vietnam); [Xuan-Tu Tran](#) (Vietnam National University, Hanoi, Vietnam)

## A2: Analog and Mixed-Signal II

### Virtual Room 1

**Session chair:** Do Anh Tuan (A\*STAR, Singapore)

**14:00 A Low-Power Low-Noise Dynamic Comparator With Latch-Embedding Floating Amplifier**

[Ziwei Li](#), [Wenbin He](#), [Fan Ye](#) and [Junyan Ren](#) (Fudan University, China)

**14:20 Capacitive recombination calibration method to improve the performance of SAR ADC**

[Hua Fan](#) (University of Electronic Science and Technology of China, China)

**14:40 A Single-Stage Delay-Tuned Active Rectifier for Constant-Current Constant-Voltage Wireless Charging**

[Xianglong Bai](#) and [Fangyu Mao](#) (University of Macau, China); [Yan Lu](#) (University of Macau, Macao); [Chenchang Zhan](#) (Southern University of Science and Technology, China); [Rui P. Martins](#) (University of Macau, Macao)

**15:00 Design of SRAM cell using Voltage Lowering and Stacking Techniques for Low Power Applications**



Jitendra Kumar Mishra (Indian Institute of Information Technology, Allahabad, India); Prasanna Kumar Misra and Manish Goswami (Indian Institute of Information Technology, India)

**15:20 *Dynamic Reduction of Power Consumption in Direct-RF Sampling Receivers with Variable Decimation***

Yuka Nakamatsu and Takao Kihara (Osaka Institute of Technology, Japan)

## D2: Digital Circuits and Systems II

### Virtual Room 2

**Session chair:** Chien-Ming Wu, (National Chip Implementation Center, NARL, Taiwan)

**14:00 *High-Performance Implementation of Adaptive IQ Mismatch Compensator in Direct-Conversion Transceiver***

Toan Van Nguyen (Viettel High Technology Industries Corporation (VHT), Viettel Group, Vietnam); Viet-Son Bui (Viettel High-Tech Industries Corporation (VHT), Vietnam); Kien Nguyen (Viettel IC, Vietnam)

**14:20 *Stress evolution analysis of EM-induced void growth for multi-segment interconnect wires***

Zaiyong Liu, Haibao Chen and Tianshu Hou (Shanghai Jiao Tong University, China)

**14:40 *Performance Analysis of Non-Profiled Side Channel Attacks Based on Convolutional Neural Networks***

Ngoc-Tuan Do and Van-Phuc Hoang (Le Quy Don Technical University, Vietnam); Sang Van Doan (Vietnam Naval Academy, Vietnam & ICT CRC, Kumoh National Institute of Technology, Korea (South))

**15:00 *An Energy-Efficient Time-Domain Binary Neural Network Accelerator with Error-Detection in 28nm CMOS***

Yuxuan Du, Xinchao Shang and Weiwei Shan (Southeast University, China)

**15:20 *Low-Power Implementation of a High-Throughput Multi-core AES Encryption Architecture***

Pham- Khoi Dong (VNU University of Engineering and Technology, Vietnam); Hung K. Nguyen (VNU University of Engineering and Technology, Vietnam); Van-Phuc Hoang (Le Quy Don Technical University, Vietnam); Xuan-Tu Tran (Vietnam National University, Hanoi, Vietnam)

## A3: Analog and Mixed-Signal III

### Virtual Room 1

**Session chair:** Chun-Lin Ko (Taiwan Semiconductor Research Institute, Taiwan)

**16:00 *Sub-Sampling Phase-Locked Loop with Ultra-mini Dead Zone For Locking Time Reduction***

Yeqing Wang and Zhouchen Ma (Shanghai Jiao Tong University, China); Lei Zhang and Zongmin Wang (Beijing Micro-electronic Technology Institute, China); Yan Liu and Jian Zhao (Shanghai Jiao Tong University, China)

**16:20 Low Power Reference Voltage Buffer and High Density Unit capacitor in a 12b 200MS/s SAR ADC**

Wenbin He, Ziwei Li, Fan Ye and Junyan Ren (Fudan University, China)

**16:40 Open Top Socketed Evaluation Board for Bench Test and Fault Localization on GaAs RF Device**

Alex Marianne A. del Castillo (Analog Devices Inc., Philippines); Ramon Garcia and Febus Reidj G. Cruz (Mapua University, Philippines)

**17:00 A Self-coupled DT MASH  $\Delta\Sigma$  Modulator with High Tolerance to Noise Leakage**

Gaofeng Tan (Shanghai Jiao Tong University, China); Haolin Lu (Tianjin University, China); Xinyu Qin, Jiliang Zhang, Jingying Zhang and Yan Liu (Shanghai Jiao Tong University, China); Liang Qi (Shanghai Jiaotong University, China)

**17:20 "Truth from Practice, Learning beyond Teaching" Exploration in teaching Analog Integrated Circuit**

Hua Fan (University of Electronic Science and Technology of China, China)

## C1: Communication Circuits and Systems

### Virtual Room 2

**Session chair:** Hsu-Feng Hsiao (National Chiao Tung University, Taiwan)

**16:00 100 MHz Random Number Generator Design Using Interleaved Metastable NAND/NOR Latches**

Chua-Chin Wang and Shao-Wei Lu (National Sun Yat-Sen University, Taiwan)

**16:20 A RISC-V SoC for Mobile Payment Based on Visible Light Communication**

Xinchao Zhong, Chiu Wing Sham and Longyu Ma (The University of Auckland, New Zealand)

**16:40 Digital Phase Estimation through an I/Q Approach for Angle of Arrival Full-Hardware Localization**

Antonello Florio, Gianfranco Avitabile and Giuseppe Coviello (Politecnico di Bari, Italy)

**17:00 Frequency-Tunable Quasi-Elliptic Filter Using Liquid Metal**

Matthew D Brown and Carlos E. Saavedra (Queen's University, Canada)

> End of Day 1

Wednesday, December 9

## K2: Keynote 2

### Rooms: Virtual Room 1

**Session chair:** Xuan-Tu Tran (Vietnam National University, Hanoi, Vietnam)

### 9:00 *IoT and Blockchain: Technologies, Challenges, and Applications*

Prof. Ren Ping Liu (University of Technology Sydney, Australia)

## SI1: Sensors and Interfaces

### Virtual Room 1

**Session chair:** Duy-Hieu Bui (Vietnam National University Hanoi, Vietnam)

### 10:00 *Damage Position Identification of Wooden House Model Using Machine Learning*

Kohei Koike, Kenta Suzuki, Mengnan Ke, Kenjiro Mori, Takumi Ito and Takayuki Kawahara (Tokyo University of Science, Japan)

### 10:20 *A Highly Linear Amp-Less Interface Circuit for Capacitive Sensors with $\Delta\Sigma$ C-DAC*

Yuya Maekawa, Shuya Nakagawa and Hiroki Ishikuro (Keio University, Japan)

## PA1: PrimeAsia 2020 - I

### Virtual Room 2

**Session chair:** Nguyen L. K. Nguyen (University of California, Davis, USA) and Thang Bui (Stony Brook University, NY, USA)

### 10:00 *A High-Performance Symmetric Hybrid Form Design for High-Order FIR Filters*

Jinghao Ye, Masao Yanagisawa and Youhua Shi (Waseda University, Japan)

### 10:20 *Low-Noise Amplifier with Wideband Feedforward Linearisation for Mid-Band 5G Receivers*

Sarmad Ozan, Manish Nair, Tommaso Cappello and Mark Beach (University of Bristol, United Kingdom (Great Britain))

### 10:40 *Random Number Generator Based on Miniature Microbial Fuel Cells*

Celal Erbay (TUBITAK - Informatics and Information Security Research Center, Turkey); Salih Ergun (TUBITAK - Informatics and Information Security Research Center, Turkey & ERGTECH Research Center, Switzerland)

## D3: Digital Circuits and Systems III

### Virtual Room 1

**Session chair:** Michael Conrad Meyer (Waseda University, Japan)

**11:00 *A Light-Weight Timing Resilient Scheme for Near-Threshold Efficient Digital ICs***  
[Xuemei Fan](#), [Hongwei Li](#), [Qiang Li](#), [Liu Hao](#) and [Shengli Lu](#) (Southeast University, China)

**11:20 *An Efficient Accelerator of the Squaring for the Verifiable Delay Function Over a Class Group***  
[Danyang Zhu](#), [Yifeng Song](#), [Jing Tian](#) and [Zhongfeng Wang](#) (Nanjing University, China); [Haobo Yu](#) (Snap Inc., USA)

**11:40 *Fast Permutation Architecture on Encrypted Data for Secure Neural Network Inference***  
[Xiao Hu](#), [Jing Tian](#) and [Zhongfeng Wang](#) (Nanjing University, China)

## PA2: PrimeAsia 2020 - II

### Virtual Room 2

**Session chair:** [Khanh N. Dang](#) (Vietnam National University Hanoi, Vietnam)

**11:00 *3D-Modeling Dataset Augmentation for Underwater AUV Real-time Manipulations***  
[Chua-Chin Wang](#), [Chia-Yi Huang](#), [Chu-Han Lin](#), [Chia-Hung Yeh](#), [Guan-Xian Liu](#) and [Yu-Cheng Chou](#) (National Sun Yat-Sen University, Taiwan)

**11:20 *Automatic Tongue Image Segmentation Based on Thresholding and an Improved Level Set Model***  
[Hongyu Gu](#) and [Zhecheng Yang](#) (Tsinghua University, China); [Hong Chen](#) (Tsinghua, China)

**11:40 *Design and manufacture power pre-amplifier module for transmitter of ground station at S-band***  
[Ha Thi Bui](#) (VietNam Space Center & VietNam National Satellite Center, Vietnam)

## D4: Digital Circuits and Systems IV

### Virtual Room 1

**Session chair:** [Akram Ben Ahmed](#) (National Institute of Advanced Industrial Science and Technology (AIST), Japan) and [Antonello Florio](#) (Politecnico di Bari, Italia)

**14:00 *An Energy Operating System Adaptive for The Sustainable And Green Energy***  
[Yen-Bor Lin](#), [Chih-Chieh Ma](#), [Chong-Cheng Hsu](#), [Ting-Chia Ou](#), [Tsung-Chieh Cheng](#) and [Wen-Fu Chen](#) (Institute of Nuclear Energy Research, Atomic Energy Council, Executive Yuan, Taiwan)

**14:20 *High Efficient Early-Complete Brute Force Elimination Method for Security Analysis of Camouflage IC***  
[Weng-Geng Ho](#), [Chuan-Seng Ng](#), [Nay Aung Kyaw](#), [Kyaw Zwa Lwin Ne](#) and [Kwen Siong Chong](#) (Nanyang Technological University, Singapore); [Bah Hwee Gwee](#) (NTU, Singapore)

**14:40 *An Efficient FPGA Accelerator Optimized for High Throughput Sparse CNN Inference***

[Jiayu Wen](#), [Yufei Ma](#) and [Zhongfeng Wang](#) (Nanjing University, China)

**15:00 *Copper Coin over Thermal Via in PCB for Thermal Management of 12 W***

[Marcus Miguel Vicedo](#) (Analog Devices Inc., Philippines); [Febus Reidj G. Cruz](#) and [Ramon Garcia](#) (Mapua University, Philippines)

## V1: Visual Signal Processing and Communications

### Virtual Room 2

**Session chair:** Teo Tee Hui (Singapore University of Technology and Design (SUTD), Singapore)

**14:00 *Fast Object Detection on the Road***

[T. Hui Teo](#) (Singapore University of Technology and Design, Singapore); [Yi Shu Tan](#) (Singapore University of Technology & Design, Singapore)

**14:20 *Graph Saliency Network: Using Graph Convolution Network on Saliency Detection***  
[Heng-Sheng Lin](#), [Jian-Jiun Ding](#) and [Jin-Yu Huang](#) (National Taiwan University, Taiwan)

**14:40 *Improved Angle Freeman Chain Code Using Improved Adaptive Arithmetic Coding***  
[Ji-Ting Wu](#) and [Jian-Jiun Ding](#) (National Taiwan University, Taiwan)

**15:00 *Using Fully Connected and Convolutional Net for GAN-Based Face Swapping***  
[Bo-Shue Lin](#), [Ding-Wen Hsu](#), [Chin-Han Shen](#) and [Hsu-Feng Hsiao](#) (National Chiao Tung University, Taiwan)

**15:20 *Dilated Residual Convolutional Neural Networks for Low-Dose CT Image Denoising***

[Thanh-Trung Nguyen](#) (University of Engineering and Technology, VNU & Thainguyen University of Information and Communication Technology, Vietnam); [Dinh Hoan Trinh](#) (Université de Bourgogne & ImViA, France); [Nguyen Linh Trung](#) (Vietnam National University, Hanoi, Vietnam); [Tran Thi Thuy Quynh](#) (VNU University of Engineering and Technology, Vietnam); [Luu Manh Ha](#) (AVITECH & FET, University of Technology and Engineering, VNU, Hanoi, Vietnam & Erasmus MC, Rotterdam, The Netherlands)

## N1: Neural Networks and Neuromorphic Engineering

### Virtual Room 1

**Session chair:** Charlotte Frenkel (Institute of Neuroinformatics, University of Zürich and ETH Zürich, Switzerland)

**16:00 *Design of an 45nm NCFET Based Compute-in-SRAM for Energy-Efficient Machine Learning Applications***

[Chia-Heng Lee](#), [Ying-Tuan Hsu](#), [Tsong-Te Liu](#) and [Tzi-Dar Chiueh](#) (National Taiwan University, Taiwan)

**16:20 *Improvement of Generalization performance for Timber Health Monitoring using Machine Learning***

[Kenta Suzuki](#), [Kohei Koike](#), [Mengnan Ke](#), [Kenjiro Mori](#), [Takumi Ito](#) and [Takayuki Kawahara](#) (Tokyo University of Science, Japan)

**16:40 LBFP: Logarithmic Block Floating Point Arithmetic for Deep Neural Networks**

Chao Ni (Nanjing University & School of Electronic Science and Engineering, China); Jinming Lu, Jun Lin and Zhongfeng Wang (Nanjing University, China)

**17:00 A Calibration Scheme for Nonlinearity of the SAR-Pipelined ADCs Based on a Shared Neural Network**

Min Chen, Yimin Wu, Jingchao Lan, Chixiao Chen, Fan Ye and Junyan Ren (Fudan University, China)

**17:20 A lightweight Max-Pooling method and architecture for Deep Spiking Convolutional Neural Networks**

Duy-Anh Nguyen; Xuan-Tu Tran ; Khanh N. Dang (Vietnam National University, Hanoi, Vietnam); Francesca Iacopi (University of Technology Sydney, Vietnam)

**CS1: Circuits and Systems**

**Virtual Room 2**

**Session chair:** Tony Tae-Hyoung Kim (Nanyang Technological University, Singapore)

**16:00 ReRAM Device and Circuit Co-Design Challenges in Nano-scale CMOS Technology**

Lu Lu, Ju Eon Kim, Vishal Sharma and Tony Tae Hyoung Kim (Nanyang Technological University, Singapore)

**16:20 Lossless EEG Compression Algorithm Based on Semi-Supervised Learning for VLSI Implementation**

Yi-Hong Chen, Yan-Ting Liu and Tsun-Kuang Chi (Chung Yuan Christian University, Taiwan); Chiung-An Chen (Ming Chi University of Technology, Taiwan); Yih-Shyh Chiou (Chung Yuan Christian University, Taiwan); Ting-Lan Lin (National Taipei University of Technology, Taiwan); Shih-Lun Chen (Chung Yuan Christian University, Taiwan)

**16:40 A 72-nW 440-mV Time Register Using Stacked-NMOS-Switched Gated Delay Cell in Biomedical Applications**

Guowei Chen, Dang Bui and X. Yu (Graduate School of Nagoya University, Japan); Md. Zahidul Islam (Graduate School of Engineering, Nagoya University, Japan); A. Kobayashi (Graduate School of Nagoya University, Japan); Kiichi Niitsu (Nagoya University, Japan)

**17:00 Random Number Generator Based on Skew-tent Map and Chaotic Sampling**

Salih Ergun (TUBITAK - Informatics and Information Security Research Center, Turkey & ERGTECH Research Center, Switzerland); Sercan Tanriseven (ERGTECH Research Center, Switzerland)

**17:20 Experimental Cryptanalysis of No-equilibrium Chaotic System Based Random Number Generator**

Burak Acar and Tufan C. Karalar (Istanbul Technical University, Turkey)

> End of Day 2



Thursday, December 10

## S1: Digital Signal Processing

### Virtual Room 1

**Session chair:** Luu Manh Ha (Vietnam National University, Hanoi, Vietnam)

#### 9:00 *Real-Time Hardware Implementation of 3D Sound Synthesis*

Sathwik GS, Barun Kumar Acharya and Bilal Ali (National Institute of Technology Karnataka Surathkal, India); Deepu Sp (National Institute of Technology Karnataka, Surathkal, India); Sumam David S. (National Institute of Technology Karnataka, India)

#### 9:20 *Axial Resolution Enhancement of Light Sheet Microscopy via Two Light Sheet*

VanNhu Le, MinhNghia Pham and Vandang Hoang (Le Quy Don Technical University, Vietnam)

#### 9:40 *Revisit to Floating-Point Division Algorithm Based on Taylor-Series Expansion*

Jianglin Wei, Anna Kuwana and Haruo Kobayashi (Gunma University, Japan); Kazuyoshi Kubo (Oyama National College of Technology, Japan)

#### 10:00 *Missing Temperature Data Recovery Methods Based on Smoothness, Bandlimitedness and Sparseness Priors*

Chien-Cheng Tseng (National Kaohsiung University of Science and Technology, Taiwan); Su-Ling Lee (Chang-Jung Christian University, Taiwan)

## M1: Multimedia Systems and Applications

### Virtual Room 2

**Session chair:** Hoang Van Xiem (Vietnam National University, Hanoi, Vietnam)

#### 9:00 *Learning Enriched Features for Video Denoising with Convolutional Neural Network*

Xianfeng Tang and Peining Zhen (Shanghai Jiao Tong University, China); Ming Kang (Galaxycore Shanghai Limited Corporation, China); Hang Yi and Wei Wang (Beijing Institute of Astronautical Systems Engineering, China); Haibao Chen (Shanghai Jiao Tong University, China)

#### 9:20 *Histogram of Oriented Gradients Feature Extraction Without Normalization*

Ling Zhang, Wei Zhou and Xin Lou (ShanghaiTech University, China)

## C: Closing session

**Rooms: Virtual Room 1, Virtual Room 2**

**11:00** Closing speech, Best paper award, announcements

> End of Day 3